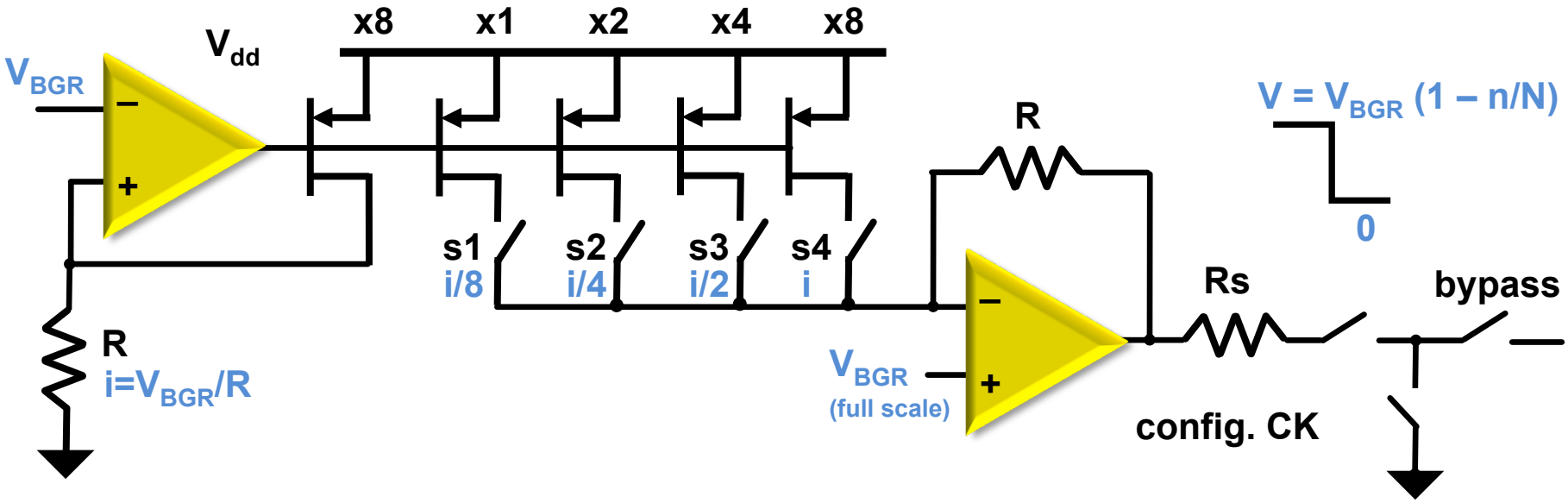
List of Changes of Cold ASICs

AUGUST 20TH, 2015

Revision Plan of Analog FE ASIC

- Revision of FE ASIC will aim to further improve the robustness of chip and simplify the system design of the front end readout electronics
  - Revisions are limited to fine adjustments with low risk
- List of changes
  - Improve the input protection
  - Implement smart reset
    - Use combination of CS and CK to generate reset internally
    - Eliminate the requirement of external reset pin
    - Circuit has been exercised in other ASICs (ADC, VMM etc.)
  - Improved driving capability of the last stage of shaper
  - Implement internal pulse generator
    - To perform precision charge calibration
    - External high precision calibration is still accessible by bypassing internal calibration circuit
    - External calibration pulse input becomes an option, easy to scale to larger detector
  - *Implement read back of internal serial configuration registers*

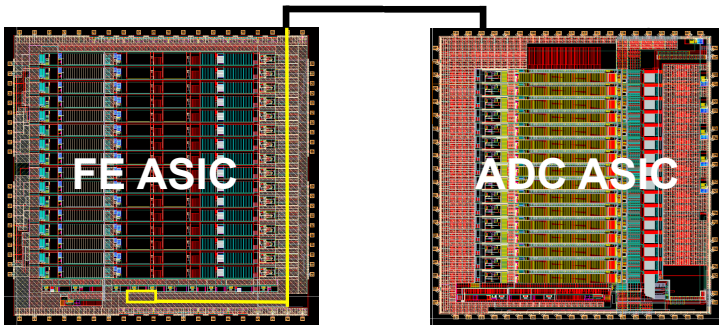
Integrated Calibration Circuit



- proven configuration, implemented in many front-end ASICs
- band-gap referenced (low temperature dependence)
- 4-bit or 5-bit programmable
- 40 mV to 1.2 V, 40 mV steps (>= 4 points per gain)
- non-linearity < 0.5 %, non-uniformity < 2 %
- re-usage of amplifiers (low risk implementation)
- re-usage of signals (config. clock)
- fully compatible with present scheme and pinout
- connect 8 FE-ASICs to reduce dispersion
- can be routed to calibrate ADCs as well

measured

$V_{BGR} \approx \begin{cases} 1.185\ V & \text{at } 300\ ^{\circ}K \\ 1.164\ V & \text{at } 77\ ^{\circ}K \end{cases}$



Revision Plan of ADC ASIC

- Revision of ADC ASIC will aim to further improve the performance, simplify the usage and interface to the front end readout electronics
  - Revisions will be based on the test results of the current version and the discussion of COLDATA interface in July
- List of changes
  - Implement the power on default configuration
  - Improve the input protection
  - Improve the ADC DNL/INL performance
  - Implement user friendly interface
    - Add dedicated test pattern generation command instead of using SDI input
  - Implement compatible SPI interface between FE ASIC and ADC ASIC
    - Future design will have a pair of FE ASIC and ADC ASIC daisy chained together
    - Both chips will use single ended signals
  - *Implement compatible interface to COLDATA ASIC*
    - *Implement ADC_CONV input and ADC_BUSY output*
  - *Implement read back of internal serial configuration registers*